In the Abstract:

~~Field-effect transistor with local source/drain insulation and associated fabrication method~~

~~The invention relates to a field-effect transistor with local source/drain insulation and to an associated fabrication method, a source depression (SV) and a drain depression (DV) being formed in a manner spaced apart from one another in a semiconductor substrate (1) and a depression insulation layer (VI) being formed at least in a bottom region of the source and drain depressions (SV, DV) and an electrically conductive filling layer (F), for realizing source and drain regions (S, D), filling the source and drain depressions (SV, DV). Together with a gate dielectric (3) and a gate layer (4), a field-effect transistor with reduced junction capacitances is obtained in this way.~~

~~Figure 1~~

A field-effect transistor (FET) with local source-drain insulation is described. The FET includes a semiconductor substrate, source and drain depressions, a depression insulation layer, an electrically conductive filling layer, a gate dielectric, and a gate layer. The depression insulation layer is formed at least in bottom regions of the source and drain depressions. The electrically conductive filling layer realizes source and drain regions and fills the source and drain depressions at a surface of the depression insulation layer. The gate dielectric is formed at a substrate surface between the source and drain depressions. The gate layer (is formed at a surface of the gate dielectric. The source and drain depressions have, in an upper region, a widening with a predetermined depth for realizing defined channel connection regions.